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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,407	07/29/2003	Jae-Soon Lim	5649-1132	7226

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MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 12/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,407	LIM ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *24-31* is/are allowed.

6)☒ Claim(s) *1-11,14-23 and 32* is/are rejected.

7)☒ Claim(s) *12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/629,407. Currently, claims 1–30 are pending.

Specification

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. *Claims 1-3, 7, 8, 10, 11, 14-16, 20, 21, and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishitani (US 5,677,226).*

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. *Claims 1-3, 5, 7, 8, 10, 11, 14-16, 18, 20, 21, 23, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishitani (US 5,677,226) in view of Wolf et al. (Silicon Processing for the VLSI Era – Vol. 1: Process Technology).*

Ishitani discloses a method of forming a capacitor (fig. 1 and accompanying text). The method comprises the following steps: forming a first conductive layer 3 on a substrate 1 (fig. 1 and col. 4, lines 14-23); forming a reaction-preventing layer 4 on the first conductive layer to prevent an oxidation of the first conductive layer (fig. 1, col. 4, lines 14-23, and col. 4, lines 53-58); forming a dielectric layer 5 on the reaction preventing layer (fig. 1 and col. 4, lines 14-23); and forming a second conductive layer 6 on the dielectric layer (fig. 1 and col. 4, lines 14-23).

The first conductive layer is a polycrystalline silicon layer (fig. 1 and col. 4, lines 14-23).

The reaction-preventing layer is a silicon nitride layer (fig. 1, col. 4, lines 14-23, and col. 4, lines 53-58).

The dielectric layer is a metal oxide layer (fig. 1 and col. 4, lines 14-23). The metal oxide layer is a $BaTiO_3$ layer, or an $SrTiO_3$ layer (fig. 1, col. 4, lines 14-23, and col. 5, lines 44-48).

The second conductive layer is a polycrystalline silicon layer (fig. 1 and col. 4, lines 14-23).

Ishitani does not teach that the nitride reaction-preventing layer is formed at a temperature below a minimum temperature associated with a phase change of the lower electrode, or that the nitride reaction-preventing layer is formed at a temperature of about 600°C or less using a chemical vapor deposition process and/or an atomic layer deposition process.

Wolf teaches forming a silicon nitride layer at a temperature of about 600°C or less using a plasma-enhanced chemical vapor deposition (PECVD) process (pages 193-194).[1] A silicon nitride layer formed at a temperature of about 600°C or less using PECVD has good step coverage (page 192 - Table 3).

In Ishitani, the lower electrode comprising the first conductive layer 3 has a contoured shape (fig. 1). One having ordinary skill in the art would have been motivated to modify Ishitani in view of Wolf by forming the silicon nitride reaction-preventing layer 4 at a temperature of about 600°C or less using a PECVD process, as taught by Wolf, since the silicon nitride layer is conformal and, thereby, conforms to the lower electrode's contoured shape.

5. *Claims 4, 6, 17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishitani in view of Wolf, as applied to claims 3 and 16 above, and further in view of Wang (US 2003/0134486 A1).*

Ishitani does not teach forming the reaction-preventing layer using a plasma nitration process, or a microwave-type deposition method.

Wang teaches forming a silicon nitride layer 16 using one of plasma nitridation, chemical vapor deposition, and remote plasma nitridation, which is a microwave-type process (fig. 2 and par. 21, lines 1-7).

Since direct plasma nitridation and remote plasma nitridation are known methods for depositing silicon nitride, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Ishitani and Wolf in view of Wang by forming the silicon nitride reaction-preventing layer using one of the two methods.

6. *Claims 9 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishitani in view of Wolf, as applied to claims 7 and 20 above, and further in view of Joo et al. (US 5,843,818).*

As discussed above, Ishitani teaches forming the dielectric layer of an $SrTiO_3$ layer. However, Ishitani does not teach that the $SrTiO_3$ layer is formed at a temperature of about 600°C or less using a chemical vapor deposition process and/or an atomic layer deposition process.

Joo teaches forming an $SrTiO_3$ layer at a temperature of about 600°C or less using a metal organic chemical vapor deposition (MOCVD) process (col. 5, lines 51-56).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the $SrTiO_3$ using the process of Joo, since it is

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[1] Polysilicon does not undergo a phase change at a temperature of 600°C or less.

a low temperature process, thereby not subjecting the structure to high temperatures which may cause damage.

Allowable Subject Matter

7. Claims 24-31 are allowed. Claims 12 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not anticipate, teach or suggest a method of forming a capacitor substantially as claimed, wherein the method comprises forming the reaction-preventing nitride layer on a cylindrical lower electrode.

Response to Arguments

Applicant's arguments filed 07 September 2004 have been fully considered but they are not persuasive. Applicant argues that the Ishitani patent does not teach the limitation of forming the silicon nitride protection layer at a temperature below a minimum temperature associated with a phase change of the lower electrode. As discussed above, Wolf teaches forming a silicon nitride layer at a temperature of about 600°C or less. Since polysilicon does not undergo a phase change at a temperature of 600°C or less, Wolf clearly teaches the limitation of forming the silicon nitride protection layer at a temperature below a minimum temperature associated with a phase change of the lower electrode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
13 December 2004

Mary Wilczewski
Primary Examiner